Specification Amendments

Please replace paragraph 0010 with the following rewritten paragraph:

0010 In a first embodiment, the method includes providing a semiconductor substrate including a polysilicon or metal gate structure including at least one overlying hardmask layer; forming spacers selected from the group consisting of oxide/nitride and oxide/nitride/oxide layers adjacent the polysilicon or metal gate structure; removing the at least one overlying hardmask layer to expose the polysilicon or metal gate structure; carrying out an ion implant process; carrying out at least one of a wet and dry etching process to reduce the width of the spacers; and, forming at least one dielectric layer over the polysilicon or metal gate structure and spacers in one of tensile and compressive stress.

Please replace paragraph 0020 with the following rewritten paragraph:

0020 Referring to figure 1C, in one embodiment of the invention, an oxide layer, for example LPCVD TEOS oxide is first blanket deposited, for example having a thickness less than about 200 Angstroms, more preferably less than about 150 Angstroms,

followed by deposition of a nitride layer, for example silicon nitride or silicon oxynitride (e.g., SiON), preferably silicon nitride, (e.g., Si_3N_4, SiN), preferably by an LPCVD process and preferably having a thickness of greater than about 450 Angstroms. A conventional wet and/or dry etchback process is then carried out to etch through a thickness of the nitride layer and underlying oxide layer to stop on the hardmask portion 16A to form nitride spacer portion e.g., 18[[A]]B and oxide spacer portion e.g., 18[[B]]A adjacent either side of the gate structure.

Please replace paragraph 0027 with the following rewritten paragraph:

0027 Referring to Figure 3, advantageously, according to the present invention, the selected amount of stress in the channel region can be increased significantly by reduction of spacer width according to preferred embodiments. For example, shown is a data representation of a CMOS device formed with a reduced spacer width according to embodiments of the present invention. Shown on the vertical axis is a ratio of channel stress to dielectric layer stress (e.g. 28) and on the horizontal axis is shown a[[n]] spacer width formed according to preferred embodiments. Data lines A, B and C represent respective spacer widths formed for a CMOS device having respective 25 nm, 40 nm, and 80 nm gate lengths. Data to the left of line A1

(shown by directional arrow A2) represent reduced spacer widths with increased channel stress for a given dielectric layer stress according to embodiments of the present invention.

Please replace paragraph 0028 with the following rewritten paragraph:

0028 It is seen that the ratio of channel stress to dielectric layer stress (vertical axis) increases with reduced spacer width, for example increasing by up to about 60 % at line B1. Therefore, advantageously, an increased level of channel stress can be formed for a given stress level of the dielectric layer following reduced spacer width formation according to embodiments of the present invention. Formation of salicides advantageously further adds to increased channel stress while reducing S/D and SDE region electrical resistance. The increased stress in the channel region, together [[is]] with salicide formation, increases charge carrier mobility while reducing short channel effects (SCE) and increasing drive current (I_D) at smaller gate lengths.